IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Helmut Theiler	Art Unit	: 2836
Serial No.	: 10/521,931	Examiner	: Adi Amrany
Filed	: July 19, 2005	Conf. No.	: 2109
Title	: CIRCUIT ARRAY		

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REPLY BRIEF

Pursuant to 37 C.F.R. § 41.41, Appellant responds to the Examiner's Answer dated September 17, 2009, as follows:

I. Independent Claims 1-11 and 19-21 Are Patentable Over US 5,504,400 (Dalnodar).

Independent claims 1 recites, among other things:

> 1. A circuit array for controlling operation of two loads that operate with a rectified AC voltage, the circuit array comprising:
> ...
> a logic unit to generate the switch control signal based on one or more logical load control signals and the logical detection signal ...

For the purposes of this appeal only, claims 1-5 and 20 stand or fall together. The Examiner's comments regarding the foregoing features of claim 1 vis-à-vis the applied Dalnodar reference are provided below.

A: Dalnodar discloses that analog signals are passed from the phase detectors (11,12) to the diac (DC1). Each phase detector (11, 12) only handles one half of the sinusoidal waveform. Accordingly, only one diode (D11, D12) is conducting at any one time. Therefore, the outputs of the diodes are either forward biased or they are not. If the diodes are forward biased, then the diode conducts (HIGH). If the diodes are not forward biased, then the diode does not conduct (LOW). The Dalnodar diodes produce logical 0 or logical 1 outputs based on the voltages present at their inputs, and the input voltages are based on the phase of the voltage source (1). Thus, Dalnodar meets the recited limitation of a phase detection device (11,12) to output a logical detection signal that is "based on" whether the phase is positive or negative.

B: Due to the biasing of the diodes (D11, D12), the variable resistors (VR11, VR12) alternately conduct. During positive half waves, only VR11 is conducting, and during negative half waves, diode D11 prevents current from flowing through VR11 (and vice versa for VR12). Therefore, the voltage drops across VR11 and VR12 and the current through VR11 and VR12 alternate between a relative high and a relative lose.

Thus, Dalnodar meets the recited limitation of "logical load control signals" and that the switch control signal is "based on" one or more logical load control signals and the logical detection signal.

[1]

Regarding the "logical detection signal" recited in claim 1, the Examiner appears to contend that in Dalnodar, analog signals are passed from phase detectors 11, 12 to a diac DC1 (see FIGS. 4 and 5B of Dalnodar, reproduced below).

[1] Examiner's Answer, page 5.

FIG. 4

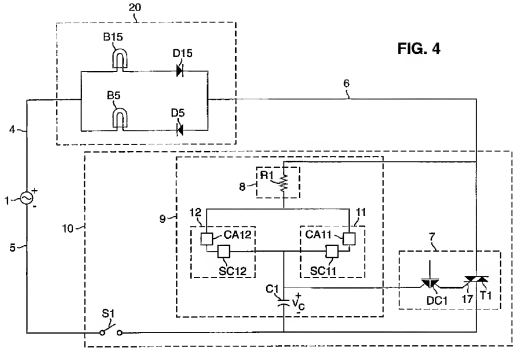
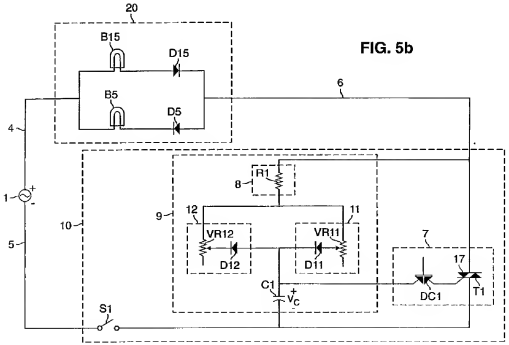

20
B15
D15
B5
D5
6
4
1
10
5
8
R1
9
12
11
CA12
CA11
SC12
SC11
C1
V_C
7
DC1
17
T1
S1

FIG. 5b


20
B15
D15
B5
D5
6
4
1
10
5
8
R1
9
12
11
VR12
VR11
D12
D11
C1
V_C
7
17
DC1
T1
S1

The Examiner further contends that because each phase detector 11, 12 only handles one half of the sinusoidal waveform, only one diode D11, D12 is conducting at any one time. As a result, the Examiner concludes that the outputs of the diodes are either operating in a HIGH state (forward biased) or in a LOW state (not forward biased), and that the resulting signal is tantamount to a logical detection signal.

Regarding the "one or more logical load control signals" recited in claim 1, the Examiner contends that due to the biasing of the diodes D11, D12, the variable resistors VR11, VR12 alternately conduct. The Examiner further contends that during respective half waves, only one of VR11 and VR12 is conducting due to the conduction of a corresponding diode D11, D12.

Stated more simply, the Examiner appears to maintain that the conducting state of the diodes and the resulting current represents the logical detection signal, and the voltage drop across the variable resistors represents the one or more logical load control signals. The Examiner appears to contend that because the variable resistors only conduct when a corresponding diode is conducting, the load control signals would be logical signals as well. We respectfully disagree.

Dalnodar is not understood to describe or suggest both a logical detection signal and one or more logical load control signals. More specifically, Dalnodar is understood to disclose passing one analog signal to the diac DC1, which the Examiner appears to concede. In this regard, the office action stated:

> The Examiner disagrees with the Appellant's interpretation of the switch control signal (Brief, pages 15-16). Claim 1 recites, in part, "a logic unit to generate the switch control signal based on one or more logical load control signals and the logical detection signal" (emphasis added). The limitation "based on" does not impart structure into the claim. Appellant's argument (Brief, page 16) that the claim calls for the use of two inputs is drawn towards unclaimed subject matter. The Examiner agrees that Dalnodar discloses one input (fig 4, 5b, horizontal line leading into the left side of item DC1). The signal at this input, however, is "based on" several factors, including the value of resistor R1, the values of resistors VR11 and VR12, the orientation of diodes D11 and D12 and the value of capacitor C1. The language of claim 1 does not require a separate input line for each of the logical load control signals and the logical detection signal. The "based on" phrase on claim 1 merely recites that the logical load control and logical detection signals have an effect on the generation of the switch control signal. This limitation is met by Dalnodar. [2]

Claim 1 clearly requires that the switch control signal be generated by the logic unit based on at least two signals, namely "one or more logical load control signals and the logical detection signal." Contrary to the Examiner's contention, the fact that a logic unit generates a switch control signal based on one or more logical load control signals and the logical detection signal does not change the fact that claim 1 requires two distinct signals.

Even if the two signals do not require two different "inputs" (as the Examiner contends), a switch control signal is still not generated based on one or more logical load control signals and the logical detection signal. For example, in Dalnodar, the signal that is derived from current passing through diode D11 via variable resistor VR11 is merely a result of the conducting state of diode D11. That is, the Examiner's interpretation of Dalnodar requires that

[2] Examiner's Answer, pages 8-9.

the signal at the input end of diode D11 be equated to the "logical load control signal," and the signal at the output end of diode D11 be equated to the "logical detection signal." Using this interpretation, it is clear that the signal has both the same "logical" state (e.g., HIGH or LOW) and the same analog value. Accordingly, the "load control signals" of Dalnodar (as suggested by the Examiner) do not comprise any information that is distinct from the information comprised by the detection signal.

Furthermore, the Examiner contends that the analog signal passing through the diodes has relatively HIGH and LOW state, thus being a logical signal. In this regard, the Examiner states:

> If the diodes are "on," then there is a current passing through the diode and the output signal is relatively HIGH (i.e. a logical "1"). If the diodes are "off," then there is no current passing through the diode and the output signal is relatively LOW (i.e. a logical "0"). Since the biasing of the diodes directly depend on the polarity of the incoming AC wave, the signals output by the diodes meet the broad limitation of being "logical." [3]

We disagree. While the signal passing through the diode may have a "HIGH" and "LOW" state relative to the "on" or "off" state of a corresponding diode, the signal itself has many intervening states (e.g., any analog value between the "HIGH" and "LOW" states). Claim 1 does not recite that the signals are logical relative to a threshold value of another component of a circuit array; rather, claim 1 recites that a logic unit generates the switch control signal based on one or more logical load control signals and the logical detection signal.

To summarize, since Dalnodar provides a single input path[4] that carries a single analog signal[5], Dalnodar neither describes nor renders obvious a logic unit to generate the switch control

[3] Examiner's Answer, page 10.
[4] The Examiner concedes this point in the Examiner's Answer, page 9. "The Examiner agrees that Dalnodar discloses one input (fig 4, 5b, horizontal line leading into the left side of item DC1). The signal at this input, however, is 'based on' several factors . . . ." *Id* (emphasis supplied).

signal based on one or more logical load control signals and the logical detection signal.

Accordingly, the rejection over Dalnodar is believed to be improper.

Claim 6

Independent claim 6 recites, among other things:

> 6. An electronic device, comprising:
> ...
> a circuit array for controlling a switch to apply voltage to first and second loads based on whether a phase of the AC voltage is positive or negative and logical load control signals generated separately for the first and second loads ...

For the purposes of this appeal only, claims 6 and 8-18 stand or fall together. The Examiner's comments regarding the foregoing claim features vis-à-vis the applied Dalnodar reference are provided below.

> With respect to claim 6, Dalnodar discloses an electronic device (figs 4-6, col 4-6), comprising:
>
> an input having leads (4, 5) to receive AC voltage (1);
>
> a circuit array for controlling a switch (T1) to apply voltage to first (B15) and second (B5) loads based on whether a phase of the AC voltage is positive (D11) or negative (D12) and load control signals (VR11-VR12) generated separately for the first and second loads, and
>
> a rectifier (D5, D15) that provides the voltage to the first and second loads, the voltage being generated from the AC voltage (1), wherein the rectifier comprises an open bridge circuit, and wherein the voltage comprises different half waves of the AC voltage, wherein a first half wave is applied to the first load and a second half wave is applied to the second load (col 3, lines 61-65).
>
> As discussed above, the diodes (D11, D12) are alternatively on (conducting) during positive and negative half waves of the incoming AC cycle. Also, the signals through the diodes and the currents/voltage drops through the resistors alternate HIGH and LOW based on whether the input is positive or negative half wave portion of the complete AC sinusoidal signal. These values meet the Applicant limitation of "logical" load control and "logical" detection signals [6]

[5] *Id.*
[6] Examiner's Answer, page 7.

As discussed above with regard to claim 1, Dalnodar neither describes nor suggests logical load control signals. In contrast to the claimed logical load control signals, Dalnodar describes an analog signal. In addition to this deficiency of Dalnodar, Dalnodar also fails to describe or to suggest that the logical load control signals are generated separately for the first and second loads.

In contrast, Dalnodar describes a single load control signal that may have either a positive or negative phase. Again, using Figure 4 of Dalnodar as an example, the load control signal is generated at capacitor C1.

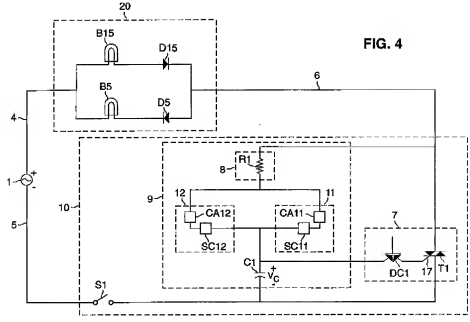


FIG. 4

The analog output of C1 flows through diac DC1 and controls the gate of triac T1. At the end of a positive cycle, the voltage of the capacitor V_c will be positive. Likewise, at the end of a negative cycle, V_c will have a negative value. Therefore, the Appellant contends that the load

control signals are not generated separately for the first and second loads; rather, Dalnodar generates a single control signal that is merely the varying value of V_c.

The Examiner contends that because the value of V_c is charged to a positive or negative value by the signal passing through either VR11 or VR12, Dalnodar discloses that the logical load control signals are generated separately for the first and second loads. However, the capacitor C1 is charged by either a positive or negative phase of the same analog signal, which results in either a positive or negative value of V_c. Thus, the control signal V_c is merely a voltage that fluctuates with varying states of the analog signal that passes through resistor R1. Accordingly, the rejection over Dalnodar is believed to be improper.

Claim 7

Claim 7 further limits the circuit array of claim 6 requiring: "a phase detection device to detect whether a phase of the AC voltage is positive or negative and to output a logical detection signal that corresponds to the phase" and "a logic unit to generate, based on the logical load control signals and the logical detection signal, a switch control signal to control the switch."

As discussed previously with regard to claim 1, Dalnodar does not describe or suggest either a logical detection signal or a logical load control signal. Accordingly, Dalnodar cannot be said to describe or suggest a logic unit to generate a switch control signal to control the switch based on those same logical signals. The Examiner's new arguments have already been addressed above with regard to claim 1. Accordingly, the rejection over Dalnodar is believed to be improper.

Claim 22

Claim 22 further limits the circuit array of claim 1 requiring that: "the logical load control signal comprises a signal selected from a group consisting of a logical 0 and a logical 1." Dalnodar neither describes nor renders obvious the features of claim 22.

In contrast to the claimed logical load control signals comprising either a logical 0 and a logical 1, Dalnodar discloses an analog signal (see discussion above in relation to claim 1). As discussed previously, while the analog signal disclosed in Dalnodar may have a value that is "HIGH" or "LOW" relative to a threshold, the signal itself (which is the claimed feature) is not a logical load control signal that comprises a signal selected from a group consisting of a logical 0 and a logical 1. The analog signal of Dalnodar does not simply alternate between a HIGH and LOW state; rather, the analog signal gradually transitions between these states by passing through a number of intervening states. Accordingly, the rejection over Dalnodar is believed to be improper.

II. Claim objections to claims 2-4, 8-10, and 22

In the current final office action, the examiner raises a new objection to claims 2-4, 8-10 and 22. In this regard the Examiner states:

> Claims 2-4, 8-10 and 22 are objected to because the word "logical" is missing before the recitations of "load control signals" and "detection signals."[7]

However, upon reading the claims, one of ordinary skill in the art would understand the subject matter of these claims. While the adjective of "logical" is not repeated in each instance of the

[7] Office Action dated May 13, 2009, page 2.

"load control signals" and "detection signals," one of ordinary skill in the art would understand that the "load control signals" and "detection signals" refer to the "load control signals" and "detection signals" of claim 1. Therefore, this objection should be withdrawn. Nevertheless, while the Appellant does not concede the appropriateness of the objection, the Appellant would consider amending claims 2-4, 8-10 and 22 at the next available opportunity.

III. Conclusion

For the foregoing reasons, and the reasons stated in the Appeal Brief, we submit that the rejections over Dalnodar should be reversed.

The undersigned attorney can be reached at the address shown below. All telephone calls should be directed to the undersigned at 617-521-7896.

The Appeal Brief fee has previously been paid. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: November 17, 2009

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